

FIG. 1

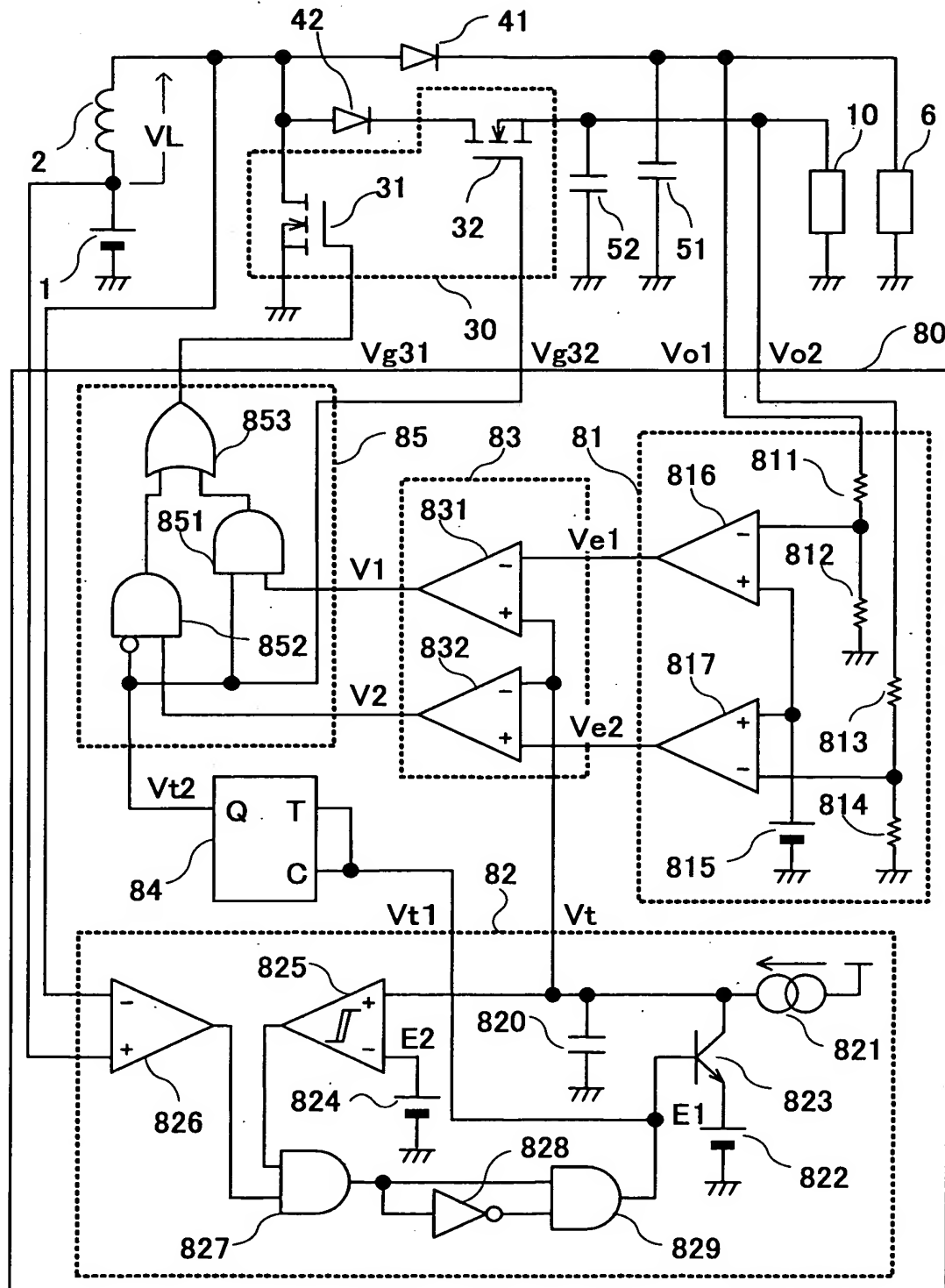


FIG. 2

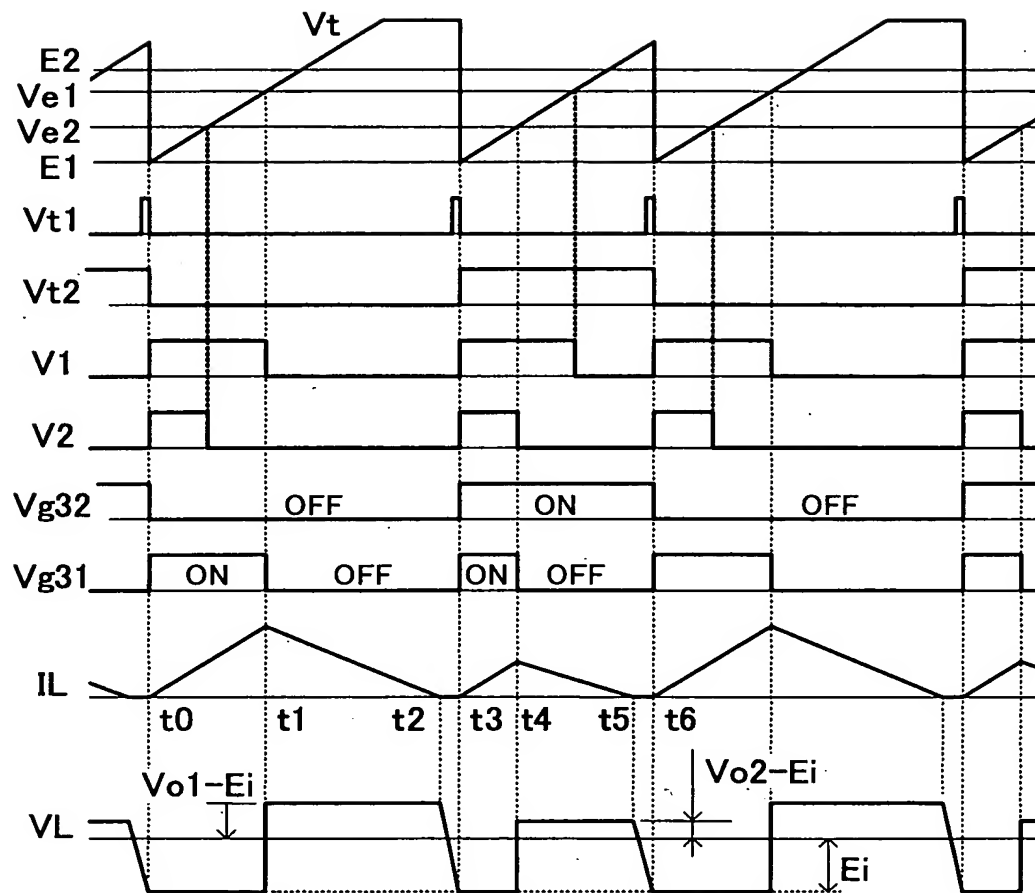
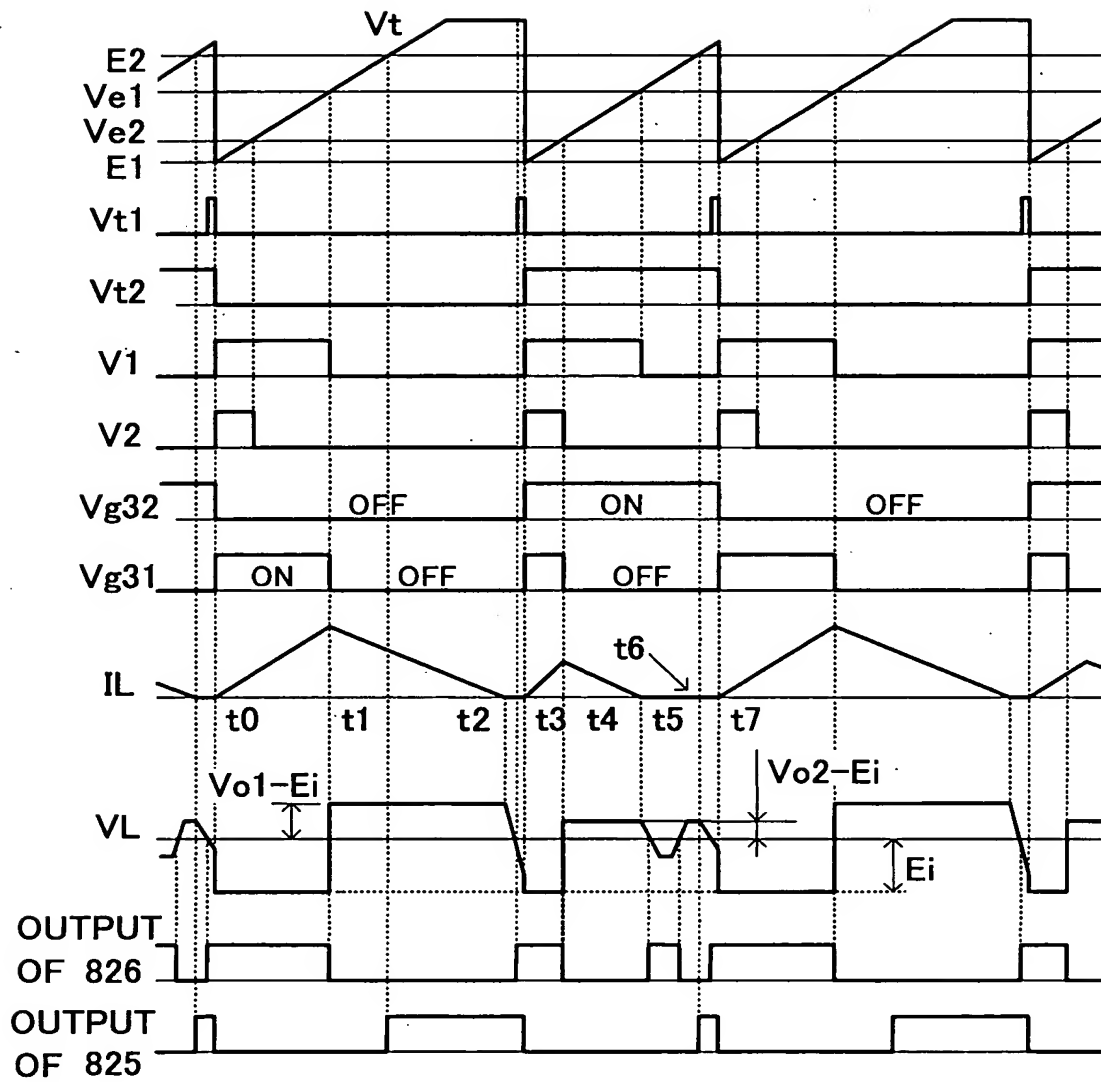


FIG. 3



The diagram illustrates a low-voltage CMOS logic circuit with a shutdown function. The circuit is divided into several functional blocks:

- Input and Biasing Section (Top):** Includes a transformer (2) and a diode (41) connected to a supply line (42). A MOSFET (31) is biased by a gate voltage  $V_{g31}$ . A second MOSFET (32) is biased by a gate voltage  $V_{g32}$ . Capacitors (51, 52) are connected to the gates of these MOSFETs.
- Logic Core (Middle):** Contains a network of CMOS logic gates (851, 852, 853, 951, 952, 953) and inverters (916, 917). The gates are interconnected to process input signals  $V_1$  and  $V_2$  into output signals  $V_{x1}$  and  $V_{x2}$ .
- Shutdown Control Section (Bottom Right):** Features a shutdown block (919) that receives a shutdown signal (918) and controls the output signals  $V_{x1}$  and  $V_{x2}$  through a network of resistors (911, 912, 913, 914) and a diode (915).
- Output and Biasing Section (Bottom Left):** Includes a MOSFET (823) and a diode (821) connected to a supply line (820). A MOSFET (822) is biased by a gate voltage  $V_{t1}$ . A MOSFET (823) is biased by a gate voltage  $V_{t2}$ . A MOSFET (824) is biased by a gate voltage  $V_{t3}$ .
- Output Section (Bottom):** The circuit outputs signals  $V_{o1}$  and  $V_{o2}$  through a network of resistors (10, 6) and a MOSFET (81).

UPPER LIMIT  
VALUE OF 1  
Vo1

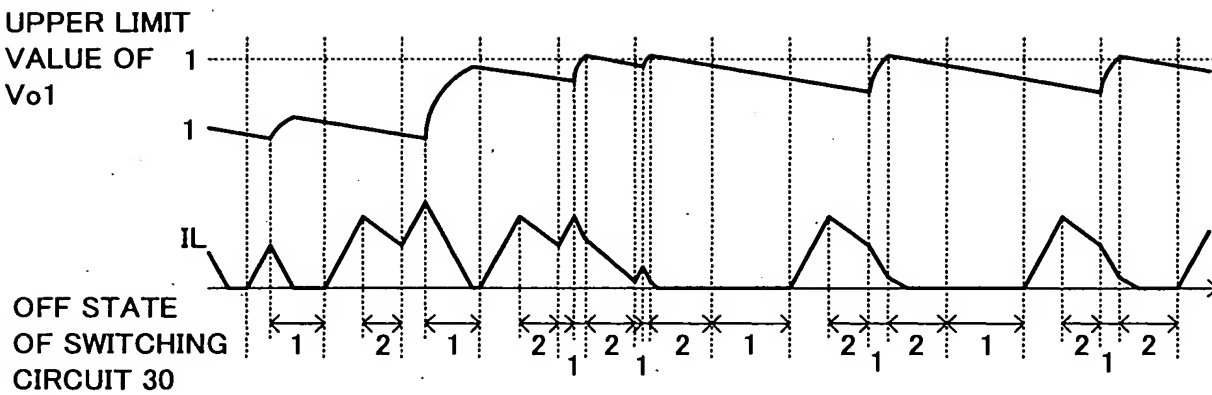


FIG. 6

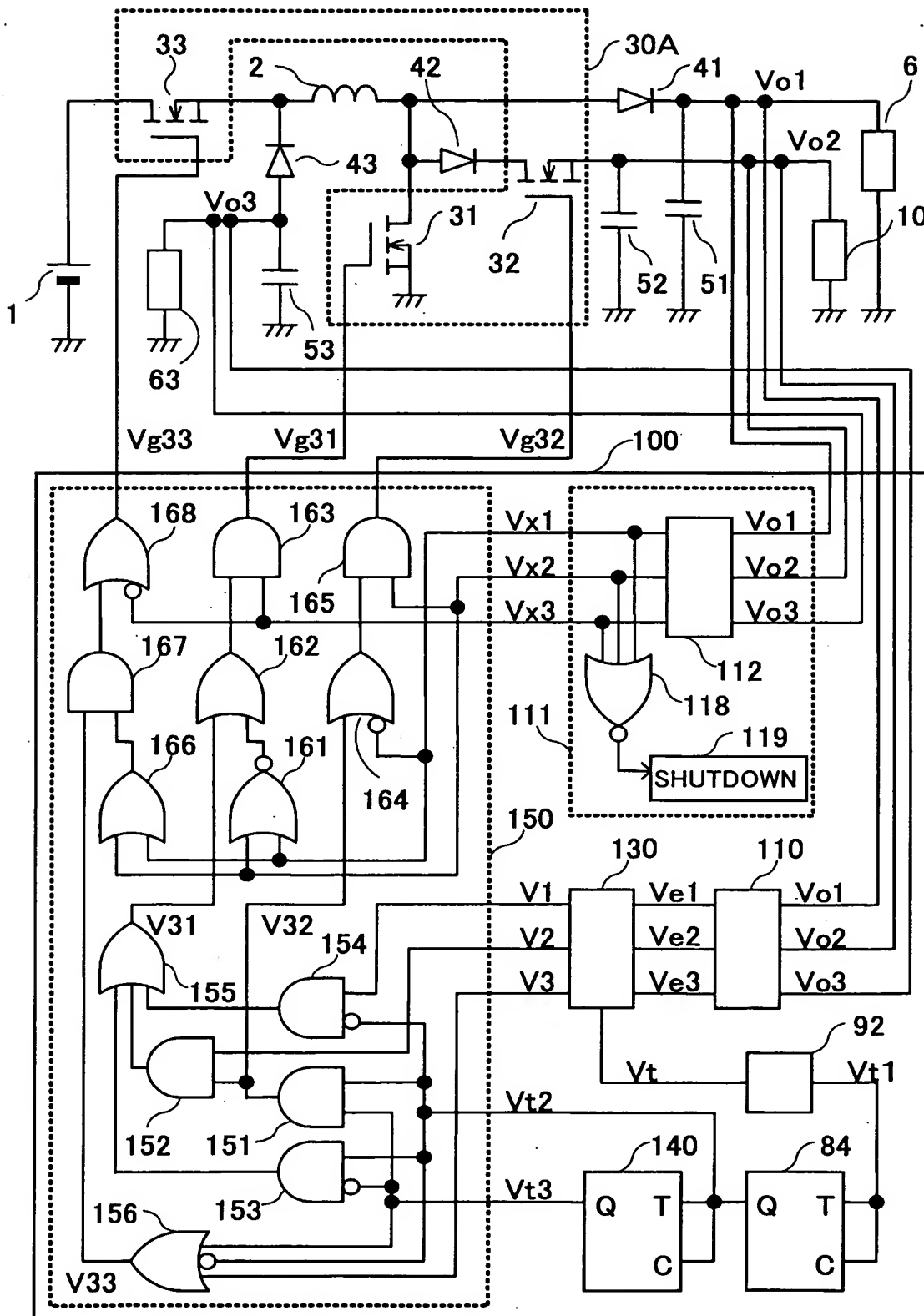


FIG. 7A

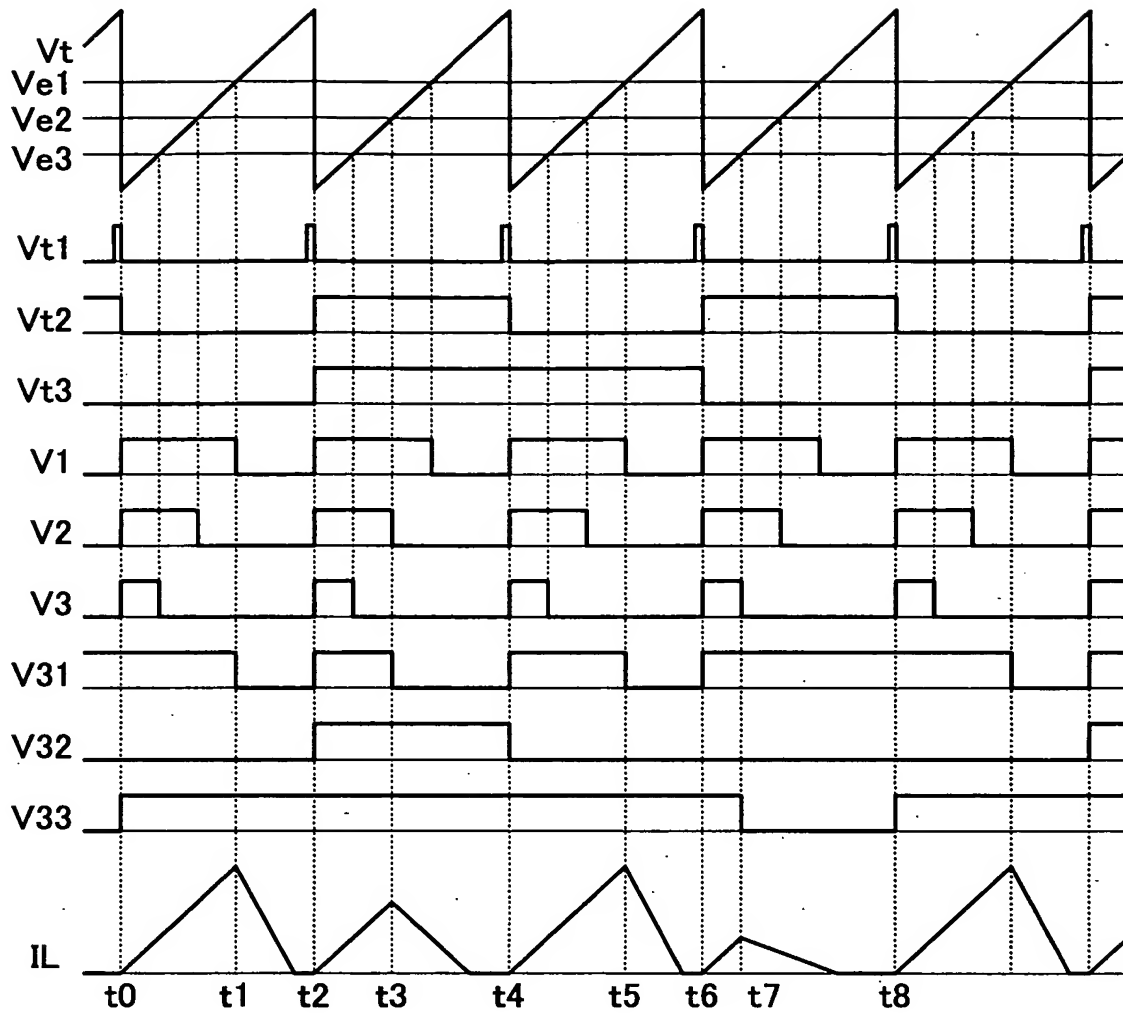


FIG. 7B

	I	II	III	IV	V	VI	VII	VIII
$V_{x1}$	H	H	H	H	L	L	L	L
$V_{x2}$	H	H	L	L	H	H	L	L
$V_{x3}$	H	L	H	L	H	L	H	L
$V_{g31}$	$V_{31}$	L	$V_{31}$	L	$V_{31}$	L	H	L
$V_{g32}$	$V_{32}$	$V_{32}$	L	L	H	H	L	L
$V_{g33}$	$V_{33}$	H	$V_{33}$	H	$V_{33}$	H	L	H

I : NORMAL OPERATION CONDITION

VIII : ABNORMAL CONDITION (SHUTDOWN)

FIG. 8

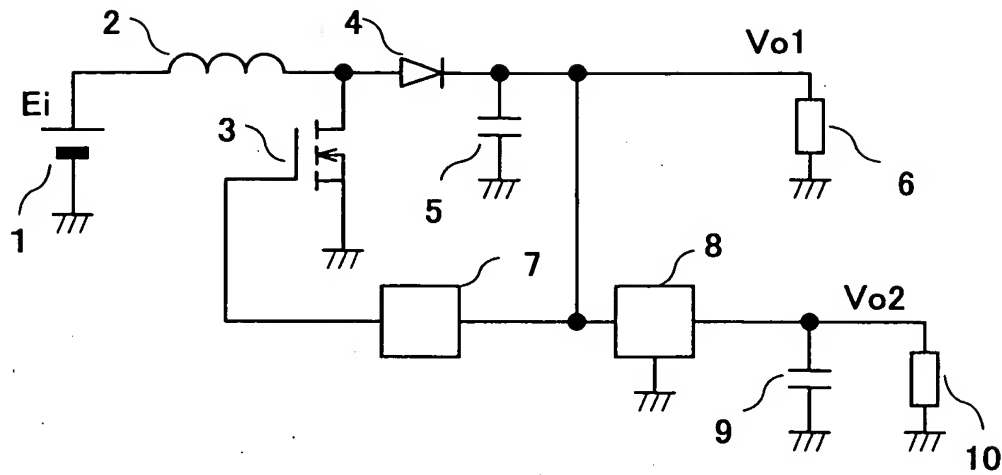


FIG. 9

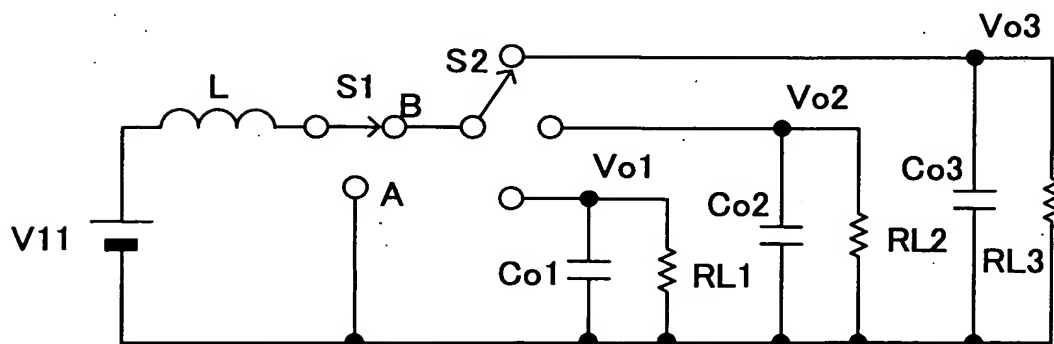




FIG. 10

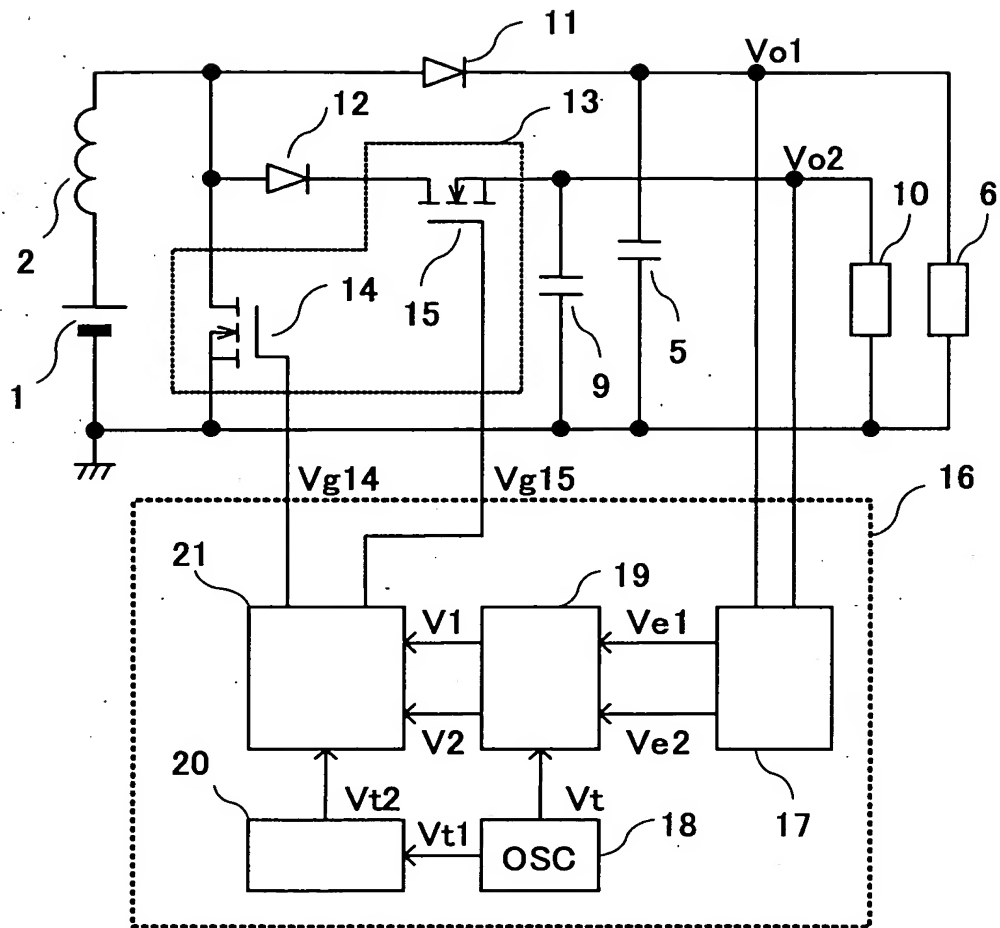


FIG. 11

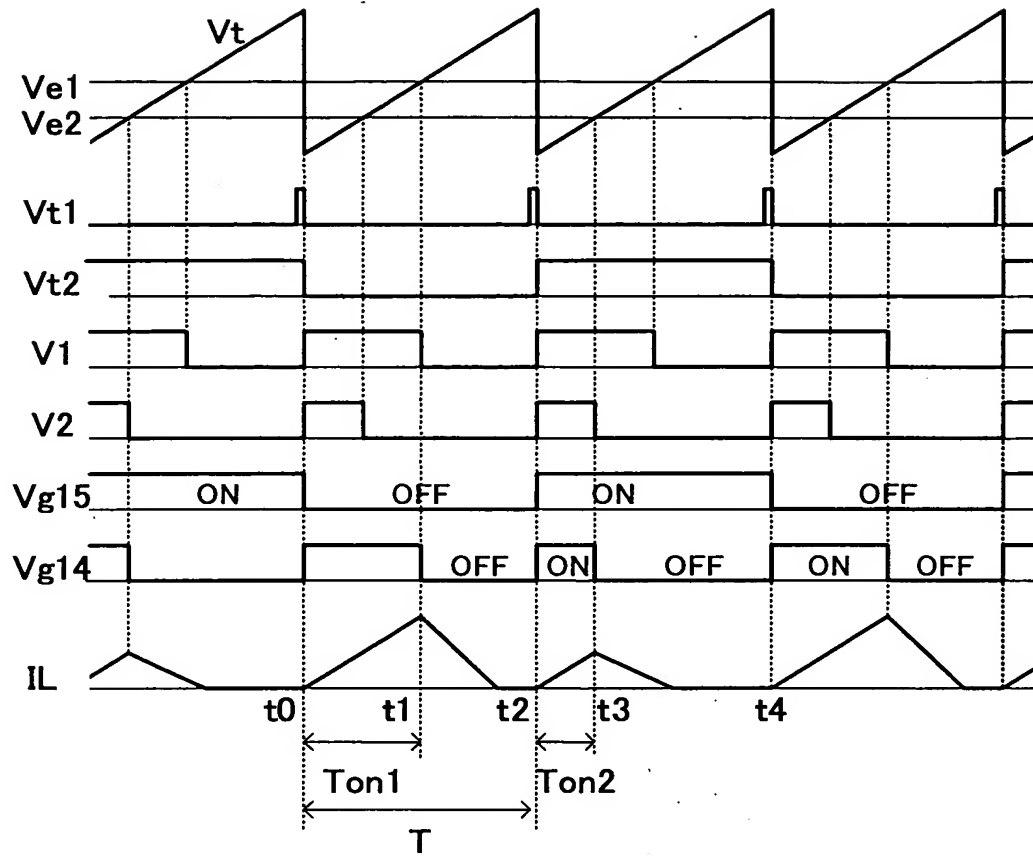


FIG. 12

